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Future developments of radiation tolerant sensors based on the MALTA architecture

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Abstract: The planned MALTA3 DMAPS designed in the standard TowerJazz 180 nm imaging process will implement the numerous process modifications, as well as front-end changes in order to boost the charge collection efficiency after the targeted fluence of 1×10^{15} 1 MeV n_{eq}/cm^2. The effectiveness of these changes have been demonstrated with recent measurements of the full size MALTA2 chip. With the original MALTA concept being fully asynchronous, a small-scale MiniMALTA demonstrator chip has been developed with the intention of bridging the gap between the asynchronous pixel matrix, and the synchronous DAQ. This readout architecture will serve as a baseline for MALTA3, with focus on improved timing performance. The synchronization

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memory has been upgraded to allow clock speeds of up to 1.28 GHz, with the goal of achieving a sub-nanosecond on-chip timing resolution. The subsequent digital readout chain has been modified and will be discussed in the context of the overall sensor architecture.

KEYWORDS: Digital electronic circuits; Electronic detector readout concepts (solid-state); Particle tracking detectors; Solid state detectors

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Contents

1 Introduction

The MALTA are a family of monolithic active pixel sensors [1] fabricated in the standard 180 nm TowerJazz imaging technology, originally designed to match the requirements of the Inner Tracker (ITk) of the ATLAS [2] experiment at the high-luminosity LHC. The main feature of this sensor is its fully asynchronous [3] matrix and readout periphery, capable of operating with hit rates up to 100 MHz. The pixels use a small collection electrode to minimize pixel capacitance. A pitch of 36.4 µm has been achieved, with an input capacitance in the order of a few femtofarads.

All MALTA sensors have been manufactured in the TowerJazz 180 nm imaging process, with additional process modifications [4, 5] developed to achieve full depletion of the sensitive layer and enhance the lateral electric field. These modifications increase the tolerance to non-ionising energy losses (NIEL) [6]. The final iteration of the front-end [7] features a cascoded charge sensitive first stage, which reduced the minimum threshold significantly. The result of these changes is the latest full scale prototype, the MALTA2, surpassing the 2×10^{15} 1 MeV n_{eq}/cm^2 NIEL requirement set by the 5th layer of the ITk of the ATLAS experiment. Due to this, further development will focus on the timing performance, as well as improving the integration capabilities of the sensor. MALTA3 will attempt to address these requirements by introducing on-chip synchronization, a revised digital periphery, and a high speed serial link for the output.

2 Current design

At their core, all MALTA sensors contain the same asynchronous matrix architecture. This matrix is structured from multiple groups of 16 pixels (2×8 layout), with a shared self-triggering reference pulse generator between them (figure 1). Each pixel contains a dual flip-flop circuit together with some input control logic, the purpose of which is to prevent the front-end from triggering more than once during the same bunch crossing. In the steady state, node MIRROR_B is set to 1. The positive edge of the pulse generated by the front end triggers the flip-flop on the right side, bringing the STATE signal to 1. The STATE signal is responsible for generating the pixel group VALID

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(preventing other pixels from generating their STATE during the current readout cycle), setting the MIRROR_B node to 0 (preventing the pixel from generating another STATE before the reset) and allowing the in-pixel address generator to transmit once the reference pulse arrives. The RESET signal is generated immediately after REF_B, resetting all active STATE signals, preparing the pixel group for the next readout cycle. The length of these two pulses can be controlled in the range of 0.5 to 2 ns. Shorter pulses are desired as the overall throughput of the matrix is increased. However, the ability to lengthen this pulse is important for maintaining proper operation of the in pixel circuitry, as well as the end of column periphery. A longer pulse avoids minimum pulse width and setup violations which might arise at higher fluences and some process corners. It must be noted that the pixel circuitry cannot generate another STATE signal until the negative edge of the front-end pulse arrives—this clears the two flip-flops, and sets the MIRROR_B node back to 1.

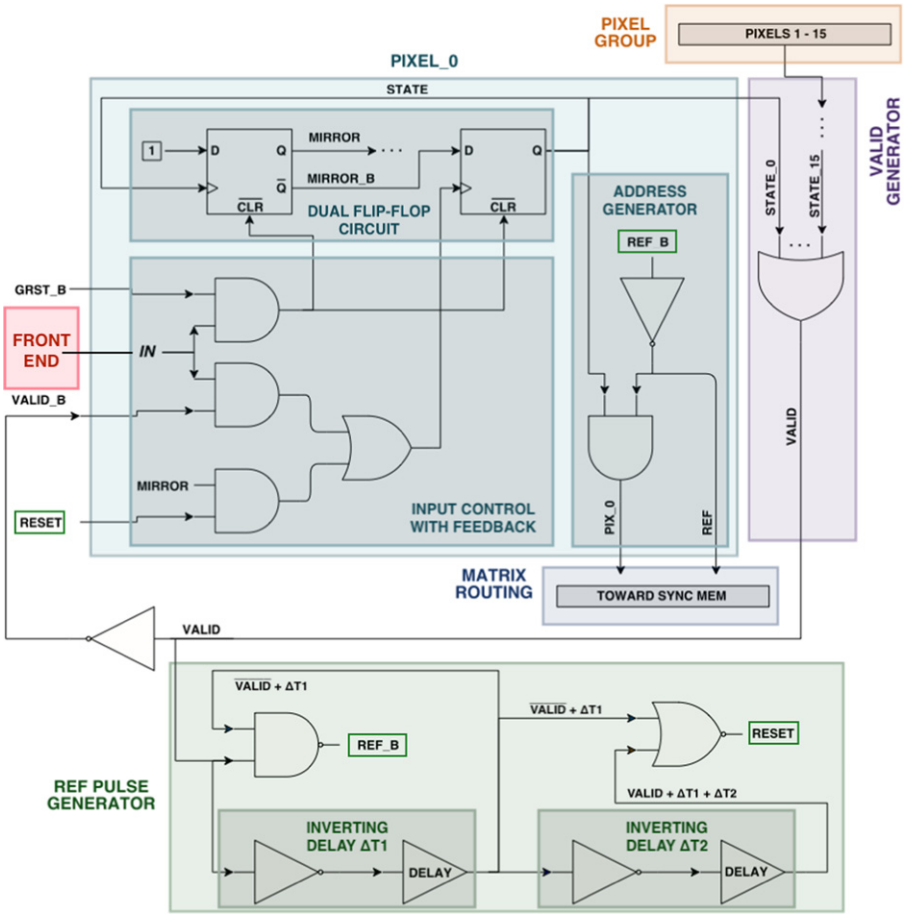

Figure 1. Pixel group circuitry block diagram.

Full size MALTA prototypes output the incoming data from the matrix using a multi-stage merging structure, ending with 40 parallel pseudo-LVDS drivers [8], designed to operate at data rates up to 5 Gbps. This approach provides minimal latency and a high output bandwidth, which is

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necessary as the timing information of the hits must be preserved up to the Data Acquisition System (DAQ). However, this approach has proved difficult to integrate in larger systems due to the need of multiple independent parallel busses. MiniMALTA, a small scale prototype with a reduced size matrix (16×64), has been developed to address this issue by time tagging incoming hits on chip. These hits, containing 22 bits each, are captured by the synchronization memory located directly below the matrix. From the 22 bits, the first one is used as a timing reference, and triggers the write operation of the corresponding SRAM cells. These synchronization memories are arrayed in groups of 4, where they share two free running counters: a 3 bit BCID (40 MHz) counter, and a 4 bit Gray counter (640 MHz). When the reference pulse is received, the current state of these counters is written together with the 21 address bits, forming a single 28 bit word. The 16 column MiniMALTA matrix requires 16 synchronization memories, one per double column group. Each memory runs completely independently, and has the capacity to store 4 events before overflowing. If a memory has events stored, a read flag becomes active. The priority encoder monitors these flags, and reads non-empty memories from left to right. An additional 9 bit address is appended in order to identify the column in which the event has happened, and the BCID is expanded to 14 bits. In total, the word is expanded to 48 bits prior to being written in the FIFO. From the FIFO, a slow or fast readout can be used to serially transmit the events off chip (figure 2).

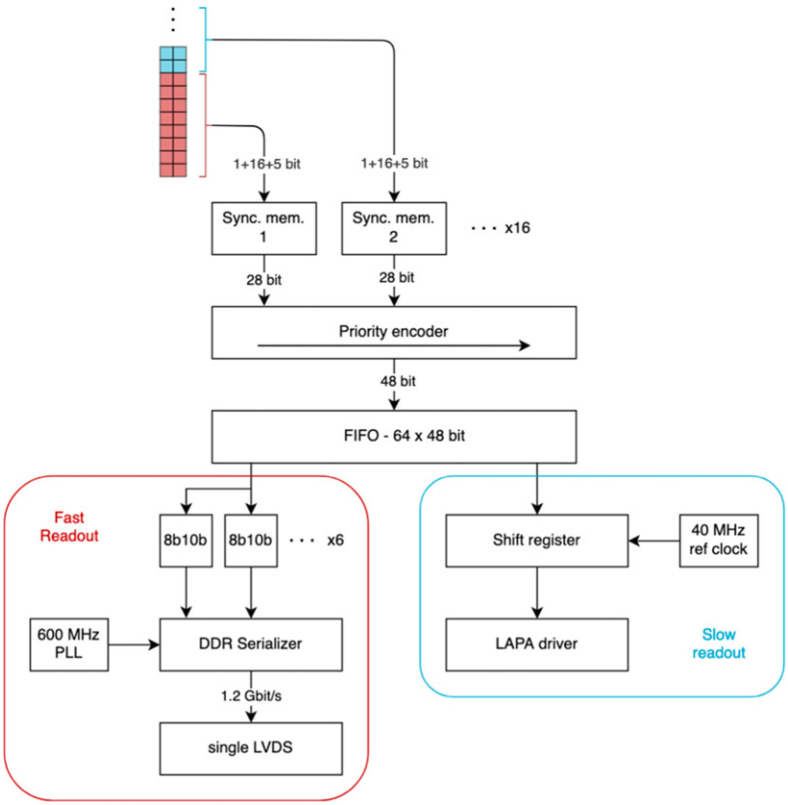

Figure 2. MiniMALTA digital periphery.

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3 MALTA3

MALTA3 [9] presents a deviation from the previous full size iterations, by expanding the on chip synchronization concept to a full scale prototype (figure 3). Minor changes to the matrix include the digital pulsing circuitry and a revised pixel masking scheme. As streamlining the integration with the DAQ is one of the main concerns of this development, supplying an external high speed clock will no longer be required due to the inclusion of a 1.28 GHz PLL. The generated clock is needed for the upgraded synchronization memory, and the output serializer. Using the MiniMALTA time tagging and readout scheme on a large matrix (768×512) presents a challenge as the individual synchronization memory module cannot serve more than 4 columns at once. A single priority encoder was enough to satisfy the reduced size matrix of the MiniMALTA, but a multi-stage FIFO based merging scheme will need to be developed for the full size prototype. This merged data stream is then to be transmitted with a single high speed serial link, using the Aurora protocol.

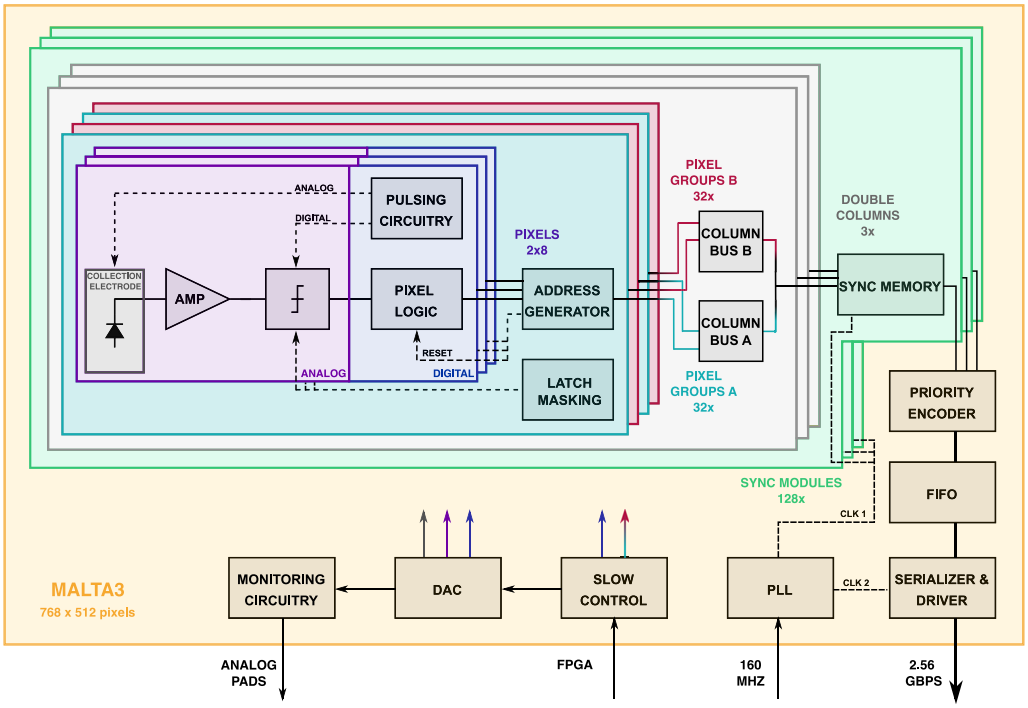

Figure 3. The proposed MALTA3 block diagram.

4 MALTA3 synchronization memory

A sub-nanosecond timing resolution has been one of the main design goals of the MALTA3. This requirement led to synchronization memory upgrades described in this section. The previous iteration was based around a 640 MHz Gray counter, designed as a single unit. Due to technology limitations, this approach was not viable at 1.28 GHz, so the module was split into two parts: a

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non-standard twisted ring counter, and a fast 16 to 5 bit Gray encoder. The twisted ring counter (figure 4) is based around repeating "bit units", consisting of an inverting D-type flip-flop and a clock NAND gate. During normal operation, the NAND functions as an inverter (RESET is set to 1), and the unit resembles a non-inverting flip flop. The counter value is tapped from the outputs of the 16 NAND gates, and is passed directly to a 4 stage Gray encoder. The reasoning behind both of these designs is a large launch delay present in the supplied flip-flops, making almost all of them non-viable for the required speed of operation.

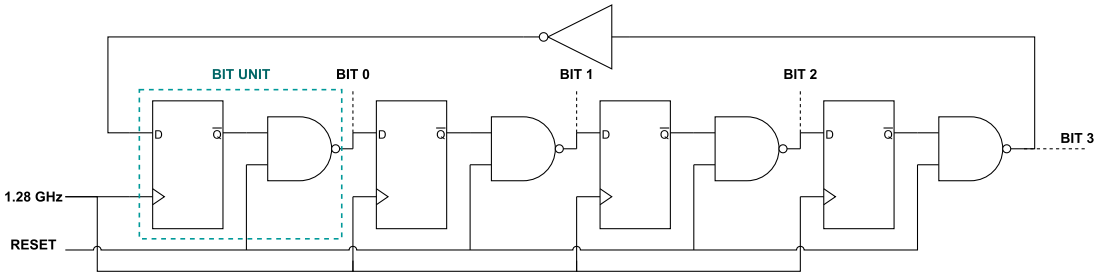

Figure 4. Architecture of the twisted ring counter used in the synchronization memory, scaled down from 16 to 4 bits.

The Gray encoded timestamp is then distributed through equal length wires towards custom SRAM cells, where it is latched using tri-state input logic (figure 5). This circuit is triggered by the same reference pulse used in the previous version of the synchronization memory. This logic was designed to eliminate the input pulse length influence on the timing resolution. Upon arrival, the reference pulse generates two signals: Primarily, it will set the W_pulse to 1, enabling the next free row of SRAM cells for writing. But before this happens, it will disable the tri-state buffers. This preserves the original values at the tri-state node, and by extension, the SRAM input. Effectively, since the value written into the SRAM cells is the one present at the end of the W_pulse, the timing and address data are latched by the positive edge of the incoming reference pulse (figure 6). Finally, the buffers are re-enabled after the write operation has finished, and the new counter value is applied at the SRAM input.

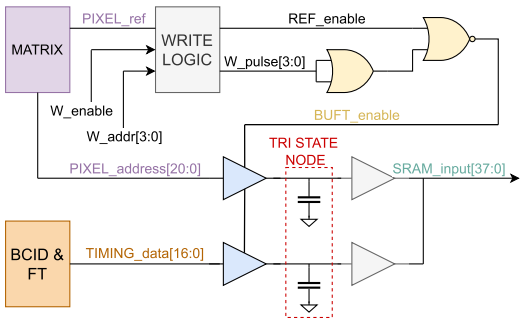

Figure 5. Tri-state input logic.

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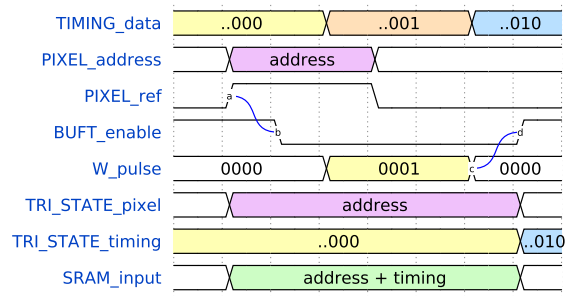

Figure 6. Timing diagram of one write operation in the synchronization memory.

5 Future outlook and conclusion

Some features of the asynchronous MALTA sensors, such as the chip to chip data transmission cannot be directly implemented with the asynchronous periphery. As this data transmission was achieved as an extension of the asynchronous merging structure already present in the chip, a new solution must be found for the new synchronous periphery. The current priority is verification of the upgraded synchronization memory, and its interaction with the newly implemented high speed serial link and Aurora encoder. For this purpose, a small scale demonstrator (MiniMALTA3) will be produced. Constructed with modularity in mind, this demonstrator will serve as the primary building block of the full size MALTA3 chip.

Acknowledgments

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